RPT5032J

The RPT5032J uses Rakon's new patented, Pluto+ ASIC. Pluto+ advances on the world famous, Pluto ASIC technology by providing enhanced frequency versus temperature stability. It also delivers to the industry the lowest jitter achievable from an ultra-stable TCXO. This allows the oscillator to comply with various standards including GR-1244, GR-253, G.812, G.813, G.8262 and G.827x.

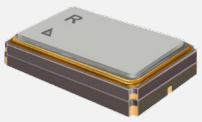
Features

- Best in-class frequency versus temperature
- RMS phase jitter down to 0.13 ps
- Phase noise < -160 dBc/Hz floor
- Excellent holdover stability

Applications

- Stratum 3 / IEEE 1588 / SyncE
- SONET / SDH / WDM / OTN
- Carrier Ethernet / Microwave
- Backhaul / Transport Equipment

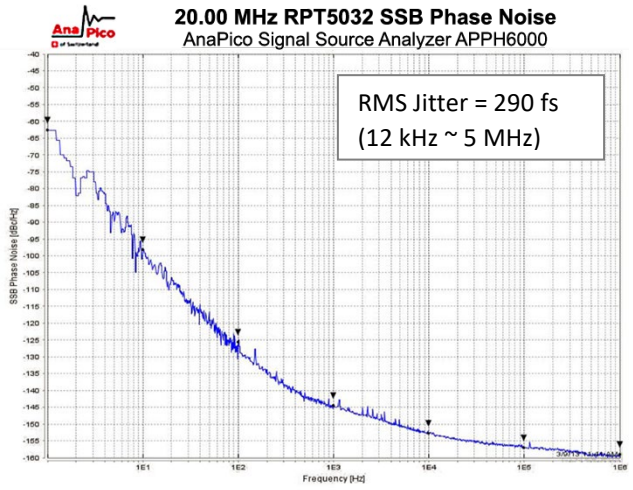
5.0 x 3.2 x 1.75 mm

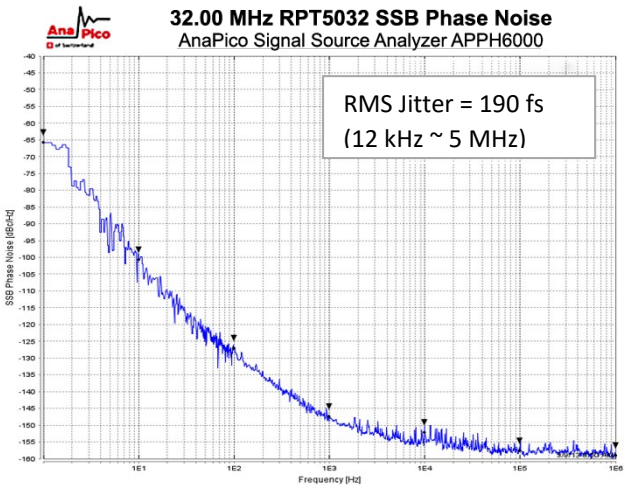


Standard Specifications

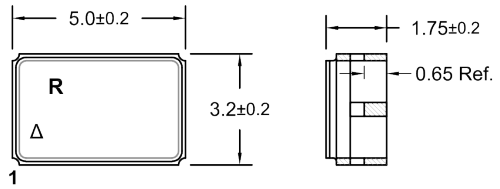
Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Nominal frequency (Fn)		10 – 40		MHz	Standard frequencies: 10, 12.8, 16.384, 19.44, 20, 20.48, 24.576, 25, 30.72, 38.88 and 40MHz
Operating temperature range	-40		85	°C	
Holdover stability, variable temperature			±100 – ±280	ppb	The default reference for holdover stability, variable temperature is (Fmax + Fmin)/2
Holdover stability, constant temperature			±10 – ±40	ppb	±10ppb after 10 days of continuous operation, ±40ppb after 48 hours of continuous operation
Slope over temperature (ΔF/ΔT)			±20 – ±100	ppb/°C	
Free-run accuracy			±4.6	ppm	Inclusive of calibration tolerance at 25°C, temperature, supply voltage variation ±5%, load variation ±5pF, reflow soldering and 20 years ageing reference to the nominal frequency
Wander generation TDEV / MTIE					TDEV compliant with GR-1244 fig 5-4, G.812 types II & III fig 2, G.813, G.8262 MTIE compliant with GR-1244 Fig 5-5, G.812 types II & III fig 1, G.813, G.8262
Supply voltage stability		±0.025		ppm	±5% variation, reference to frequency at nominal supply voltage
Acceleration stability		< 2		ppb/*g*	Gamma vector, 3-axes, 30-1500Hz
Start-up time			5 – 15	ms	90% amplitude
Root Allan Variance		5		10^{-11}	tau = 1.0s
Supply voltage, V_{CC}		3.3		V	±5%
Supply current	3		6	mA	Depending on nominal frequency
Oscillator output – HCMOS					LVCMOS & LVTTL compatible as per JESD8C
Output voltage level high (V_{OH})	$0.9V_{CC}$			V	
Output voltage level low (V_{OL})			$0.1V_{CC}$	V	
Duty cycle	45		55	%	At 50% level
Rise & fall time			8	ns	Between 10% and 90%
Load	0	15	30	pF	
Tri-state control					
Input level low (pin 6)			$0.2V_{CC}$	V	Device disabled, output in high impedance state
Input level high (pin 6)	$0.6V_{CC}$			V	Device enabled, operating

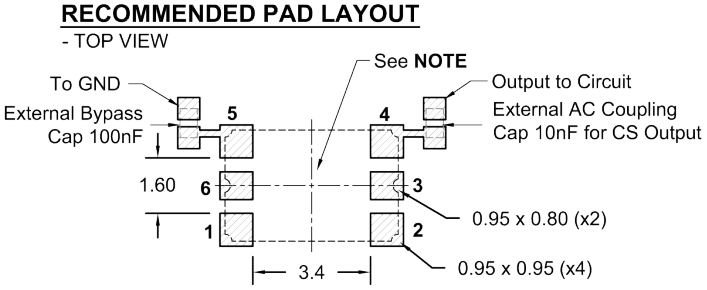
SSB Phase Noise (Typical value at 25°C)

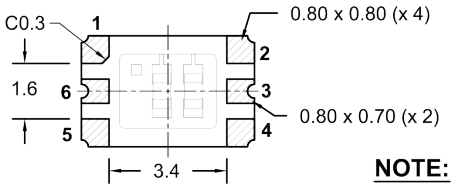




Model Outline and Recommended Pad Layout





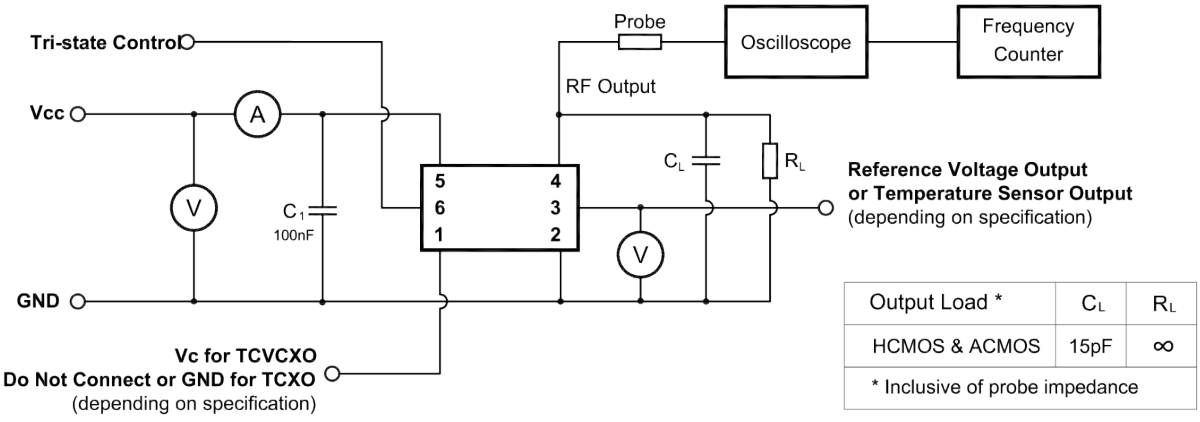


PIN CONNECTIONS	
1 * Do Not Connect / Vc	4 RF Output
2 GND	5 Vcc
3 * Do Not Connect / Vref / Vtemp	6 Enable
* Depending on specification	

NOTE:

- Unit: mm
- The area between the pads is a keep-out area, no tracks or ground plane allowed on any layer

Test Circuit



Output Load *	C_L	R_L
HCMOS & ACMOS	15pF	∞
* Inclusive of probe impedance		