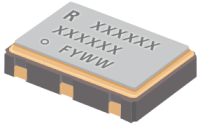
RVX5032R

SMD Voltage Controlled Crystal Oscillator



High performance VCXO in 5 x 3.2 mm Surface Mount Package

Product description

The RVX5032R VCXO combines high performance with short lead times to accelerate development and minimize inventory. 2000+ frequency configurations are available for immediate sampling and short lead-times enable reduced inventory levels.

Applications

- Basestation
- Communications
- Ethernet
- Consumer Products
- SONET/SDH
- WiMAX/WLAN

Features

- Fast sample turnaround available
- LVCMOS, LVPECL, or LVDS Output options
- Wide frequency range
- Low power differential outputs
- Small form factor

Specifications

1.0 SPECIFICATIONS REFERENCES

Line	Parameter	Description
1.1	Model Description	RVX5032R VCXO
1.2	Reference Number	
1.3	Rakon Part Number	

2.0 FREQUENCY CHARACTERISTICS

Line	Parameter	Test Condition	Value	Unit
2.1	Frequency		8 to 1500	MHz
2.2	Operating Temperature Range		-40 to 85	°C
2.3	Frequency Stability	Including Temperature range, Supply variation, Load variation & 15 years aging at 25°C	±25 to 50	ppm
2.4	Temperature Stability	Temperature range only	±10 to 20	ppm

3.0 POWER SUPPLY

Line	Parameter	Test Condition	Value	Unit
3.1	Supply Voltage (VDD)	With a tolerance of ±10%	3.3	V
3.2	Supply Voltage (VDD)	With a tolerance of ±5%	2.5	V
3.3	Supply Current	For LVCMOS (15 pF load)	30 max	mA
3.4	Supply Current	For LVPECL (50 Ω)	65 max	mA
3.5	Supply Current	For LVDS (100 Ω)	40 max	mA

4.0 CONTROL VOLTAGE (VCO)

Line	Parameter	Test Condition	Value	Unit
4.1	Absolute Pull Range (APR)		±50 min	ppm
4.2	Total Pull Range	Frequency shift from minimum to maximum control voltage	200 max	ppm
4.3	Control Voltage	Nominal 1.65V	0 to 3.3	V
4.4	Linearity	Control voltage 0.3 to 3V	15 max	%
4.5	Slope	Positive only		
4.6	Modulation BW	Control voltage 0.3 to 3V	10 min	kHz
4.7	Input Impedance		1 min	MΩ

5.0 OUTPUT CHARACTERISTICS - LVCMOS UP TO 200MHz ONLY

Line	Parameter	Test Condition	Value	Unit
5.1	Output Voltage (Vol)	15pF load	10 max	%VDD
5.2	Output Voltage (Voh)	15pF load	90 min	%VDD
5.3	Duty Cycle	@ 50% VDD	48 to 52	%
5.4	Rise Time / Fall Time	90%/10% at 15pF output load	3 max	ns
5.5	RMS Phase Jitter	Typical integrated 12 kHz to 20 MHz	0.9	ps

6.0 OUTPUT CHARACTERISTICS - LVPECL ONLY

Line	Parameter	Test Condition	Value	Unit
6.1	Output Voltage (Vol)	50Ω nominal load. (VDD - 1.6V) max.		
6.2	Output Voltage (Voh)	50Ω nominal load. (VDD - 1.03V) min.		
6.3	Duty Cycle	@ VDD - 1.3V (45 to 55% for 600 MHz+)	48 to 52	%
6.4	Output Load	With VDD -2 V	50	Ω
6.5	Rise Time / Fall Time	80%/20% at 50Ω output load	0.6 max	ns
6.6	RMS Phase Jitter	Integrated 12kHz to 20MHz	0.9	ps

7.0 OUTPUT CHARACTERISTICS - LVDS ONLY

Line	Parameter	Test Condition	Value	Unit
7.1	Differential Output: Voltage Swing (Vod)		350	mV
7.2	Duty Cycle	Measure at 1.25V (45 to 55% for 600 MHz+)	48 to 52	%
7.3	Output Load	RL = 100 Ω / CL = 10 pF		
7.4	Rise Time / Fall Time	RL = 100 Ω / CL = 10 pF	0.6 max	ns
7.5	RMS Phase Jitter	Integrated 12kHz to 20MHz	0.9	ps

8.0 SSB PHASE NOISE

Line	Parameter	Test Condition	Value	Unit
8.1	SSB Phase Noise power density @ 10 Hz offset	Typical value for a 312.5 MHz VCXO @ 25°C	-48	dBc/Hz
8.2	SSB Phase Noise power density @ 100 Hz offset	Typical value for a 312.5 MHz VCXO @ 25°C	-80	dBc/Hz
8.3	SSB Phase Noise power density @ 1 kHz offset	Typical value for a 312.5 MHz VCXO @ 25°C	-106	dBc/Hz
8.4	SSB Phase Noise power density @ 10 kHz offset	Typical value for a 312.5 MHz VCXO @ 25°C	-111	dBc/Hz
8.5	SSB Phase Noise power density @ 100 kHz offset	Typical value for a 312.5 MHz VCXO @ 25°C	-122	dBc/Hz

9.0 SSB PHASE NOISE

Line	Parameter	Test Condition	Value	Unit
9.1	SSB Phase Noise power density @ 10 Hz offset	Typical value for a 704.00 MHz VCXO @ 25°C	-46	dBc/Hz
9.2	SSB Phase Noise power density @ 100 Hz offset	Typical value for a 704.00 MHz VCXO @ 25°C	-80	dBc/Hz
9.3	SSB Phase Noise power density @ 1 KHz offset	Typical value for a 704.00 MHz VCXO @ 25°C	-98	dBc/Hz
9.4	SSB Phase Noise power density @ 10 KHz offset	Typical value for a 704.00 MHz VCXO @ 25°C	-103	dBc/Hz
9.5	SSB Phase Noise power density @ 100 KHz offset	Typical value for a 704.00 MHz VCXO @ 25°C	-103	dBc/Hz

10.0 SSB PHASE NOISE

Line	Parameter	Test Condition	Value	Unit
10.1	SSB Phase Noise power density @ 10 Hz offset	Typical value for a 61.44 MHz VCXO @ 25 °C	-78	dBc/Hz
10.2	SSB Phase Noise power density @ 100 Hz offset	Typical value for a 61.44 MHz VCXO @ 25 °C	-98	dBc/Hz
10.3	SSB Phase Noise power density @ 1 kHz offset	Typical value for a 61.44 MHz VCXO @ 25 °C	-120	dBc/Hz
10.4	SSB Phase Noise power density @ 10 kHz offset	Typical value for a 61.44 MHz VCXO @ 25 °C	-123	dBc/Hz
10.5	SSB Phase Noise power density @ 100 kHz offset	Typical value for a 61.44 MHz VCXO @ 25 °C	-122	dBc/Hz

11.0 PIN CONNECTIONS

Line	Parameter	Description
11.1	Pin 1	VCO
11.2	Pin 2	E/D* or NC
11.3	Pin 3	GND
11.4	Pin 4	OUTPUT
11.5	Pin 5	COMPLIMENTARY OUTPUT (LVPECL/LVDS only), or E/D* or NC
11.6	Pin 6	VDD
11.7	* Output Enabled	>70% of VDD on E/D pin, or E/D pin left open (connected to internal pull-up resistor)
11.8	* Output Disabled	<30% of VDD on E/D pin, or E/D pin to GND

12.0 PACKAGE DETAILS

Line	Parameter	Description
12.1	Package	F
12.2	Top line marking	[R ######] Part identifier
12.3	Middle line marking	[######] Part information
12.4	Bottom line marking	[o FYWW] Pin 1, Manufacturing code, Year code* and Week code**
12.5	* Year code	A = 2010, B = 2011, C = 2012, D = 2013, ... Z = 2035
12.6	** Week Code	WW = 01 = Week of first Monday of the year

13.0 ENVIRONMENTAL SPECIFICATIONS

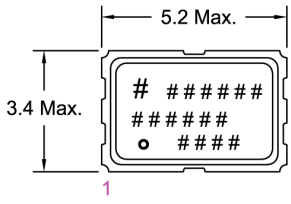
Line	Parameter	Description
13.1	Mechanical Shock	MIL-STD-883, Method 2002
13.2	Storage Temperature range	-55 to 125 °C
13.3	Thermal Shock	MIL-STD-883, Method 1011
13.4	Vibration	MIL-STD-883, Method 2007
13.5	Gross and Fine Leak	MIL-STD-883, Method 1014
13.6	RoHS Compliant	Yes

14.0 MANUFACTURING INFORMATION

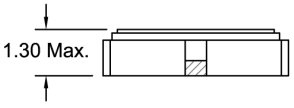
Line	Parameter	Description
14.1	Packaging Description	Tape and reel. Standard packing quantity is 4000 per reel
14.2	Reflow	Solder reflow process as per attached profile

Drawing Name: XO/VCXO 5032 6-Pin Model Drawing

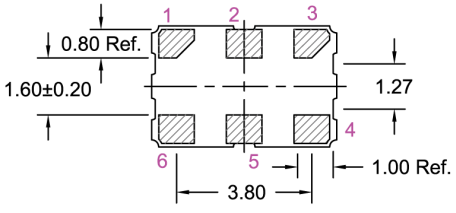
PACKAGE G65



TOP VIEW

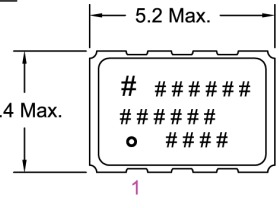


FRONT VIEW

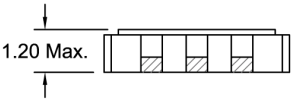


BOTTOM VIEW

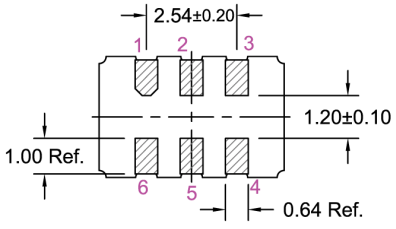
PACKAGE GV5



TOP VIEW

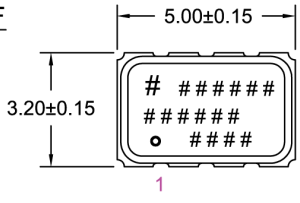


FRONT VIEW

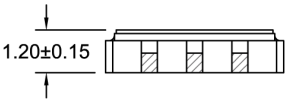


BOTTOM VIEW

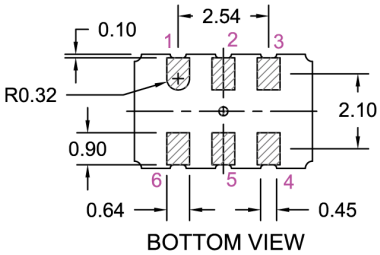
PACKAGE F



TOP VIEW



FRONT VIEW

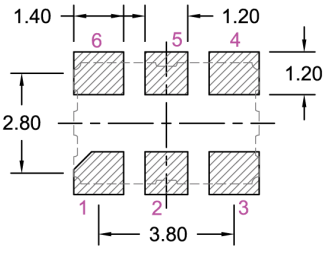


BOTTOM VIEW

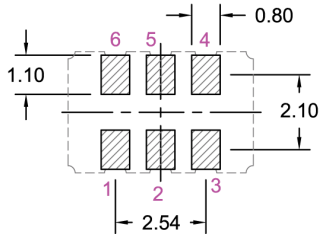
NOTE :
1. PIN CONNECTIONS ARE DETAILED IN THE SPECIFICATION.
2. MARKING INFORMATION IS DETAILED IN THE SPECIFICATION.

RECOMMENDED PAD LAYOUT - Top View

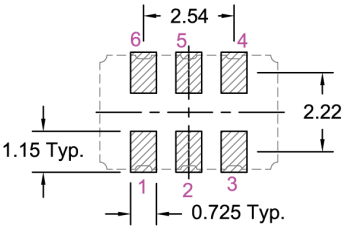
PACKAGE G65



PACKAGE GV5



PACKAGE F



TITLE: XO/VCXO 5032 6-PIN MODEL	FILENAME: CAT026	TOLERANCES:	
RELATED DRAWINGS:	REVISION: C	XX =	
	DATE: 01-May-12	X.X = ±0.15	
	SCALE: 5 : 1	X.XX = ±0.10	
	Millimetres	X.XXX =	
		X° =	
		Hole =	

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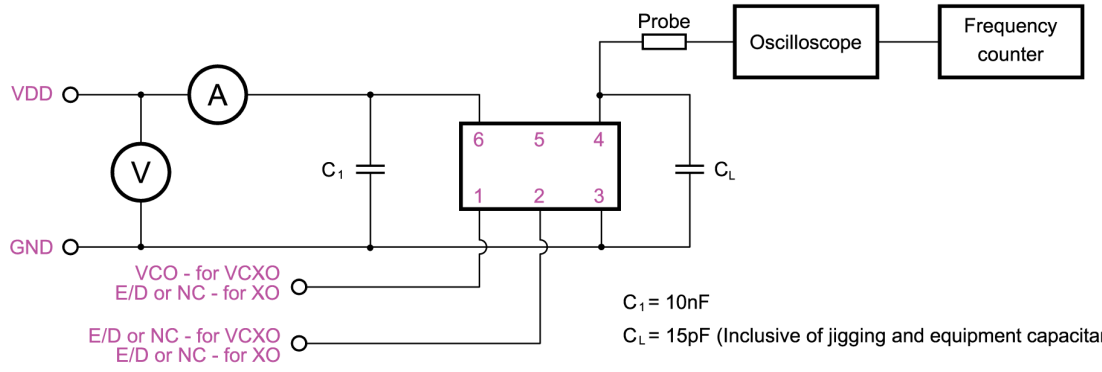
Drawing Name: XO/VCXO 6 Pin Series Test Circuit

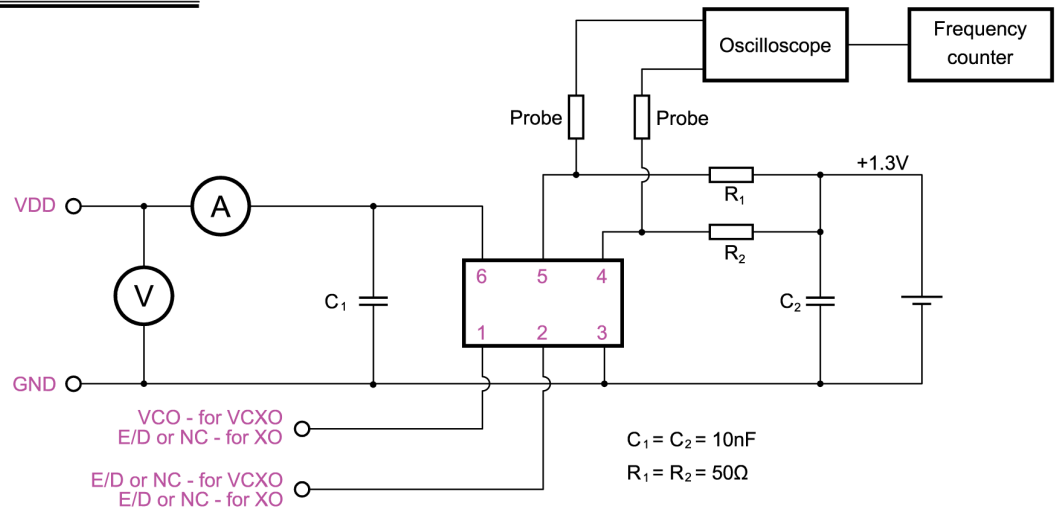
LVCMOS TEST CIRCUIT:



C_1 = 10nF

C_L = 15pF (Inclusive of jigging and equipment capacitance)

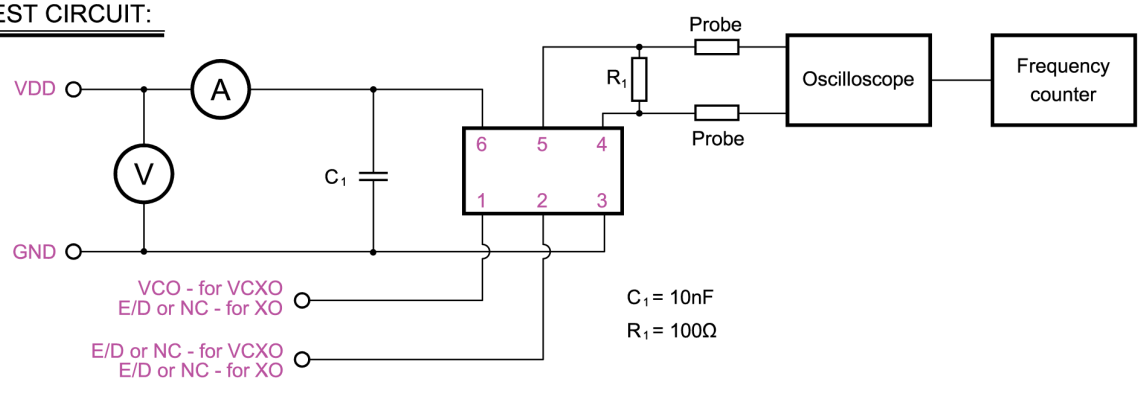
LVPECL TEST CIRCUIT:



$C_1 = C_2$ = 10nF

$R_1 = R_2$ = 50Ω

LVDS TEST CIRCUIT:



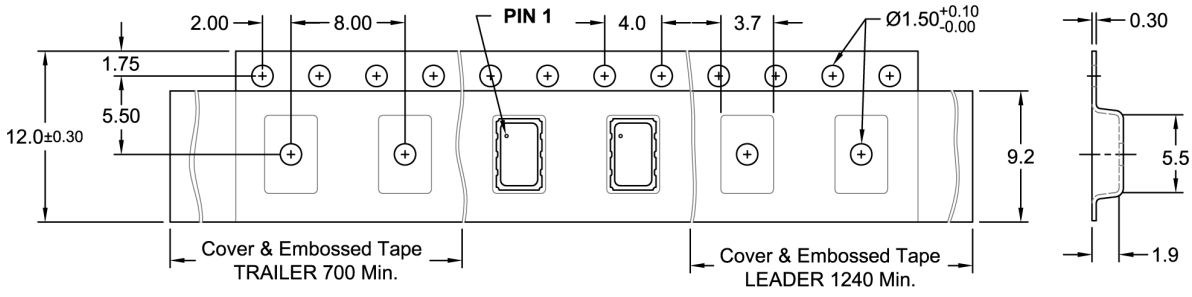
C_1 = 10nF

R_1 = 100Ω

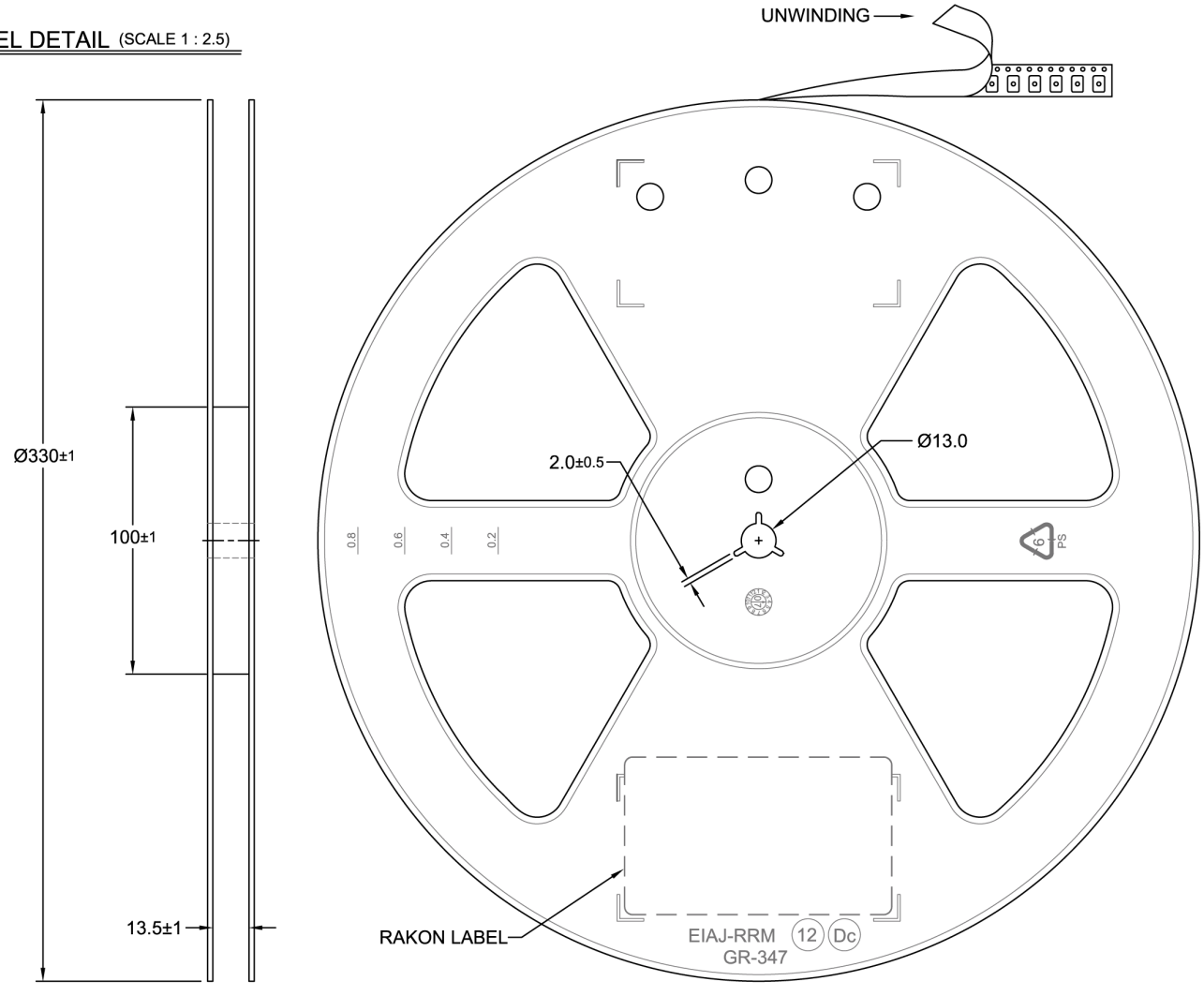
TITLE: XO/VCXO 6 PIN SERIES TEST CIRCUIT	FILENAME: CAT088
RELATED DRAWINGS:	REVISION: F
	DATE: 03-May-12
	SCALE: 1 : 1
	Millimetres

Drawing Name: XO/VCXO5032 F Series Tape & Reel

TAPE DETAIL (SCALE 2 : 1)



REEL DETAIL (SCALE 1 : 2.5)



TITLE: XO / VCXO 5032 F SERIES TAPE & REEL	FILENAME: CAT029	TOLERANCES:	
RELATED DRAWINGS:	REVISION: B	XX =	
	DATE: 14-Oct-11	X.X = ±0.1	
	SCALE: 2 : 1	X.XX = ±0.05	
	Millimetres	X.XXX =	
		X° =	
		Hole =	

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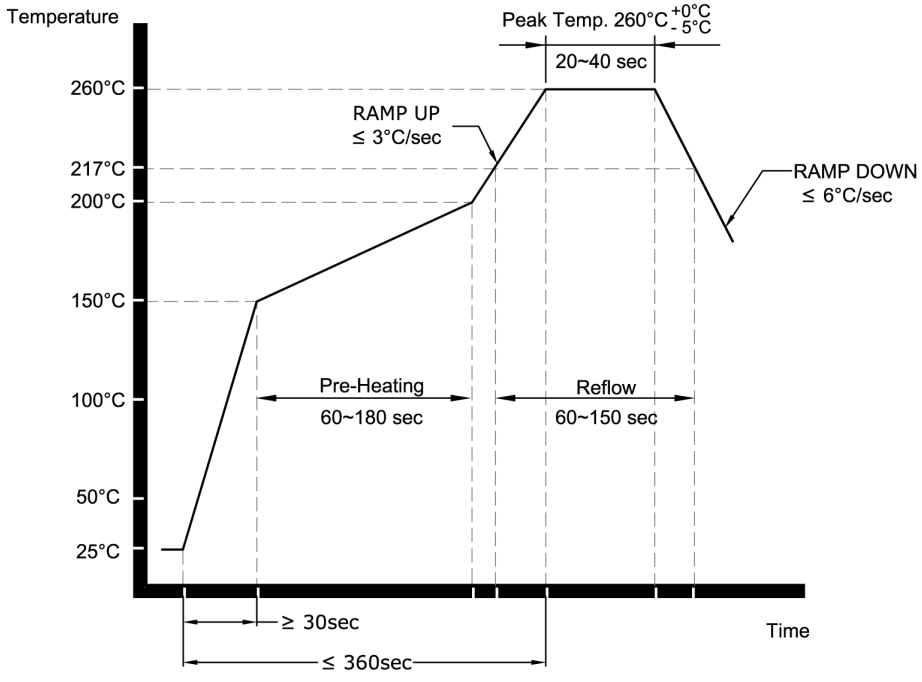
Drawing Name: Pb-Free Reflow



NOTE:
The product has been tested to withstand the Reflow Profile shown. The Reflow Profile used to solder Rakon products is determined by the solder paste Manufacturer's specification. It is recommended that the Reflow Profile used does not exceed the one shown above.

TITLE: Pb-FREE REFLOW	FILENAME: CAT541
RELATED DRAWINGS:	REVISION: B
	DATE: 05-Sep-11
	SCALE: NTS
	Millimetres