RHF7050A

The RHF7050A employs patented analogue temperature compensation to deliver tight stability down to ±0.28 ppm for high frequency differential outputs up to 1 GHz (or CMOS outputs up to 180 MHz) in a small 7.0 x 5.0 mm hermetically sealed SMD package.

Features

- CMOS, LVPECL, or LVDS output options
- Custom frequency up to 1 GHz output
- Frequency slope and perturbation specifications can be customized
- VCO tilt compensation

Applications

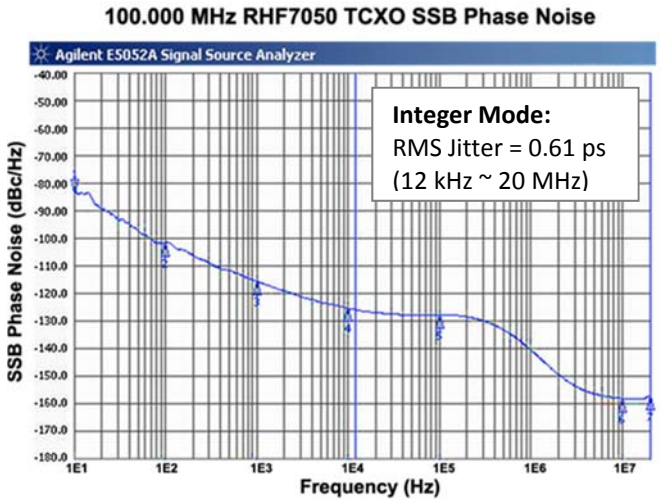
- Networking
- Base Stations
- Communications
- DSL/ADSL
- IP Timing

7.0 x 5.0 x 1.65 mm

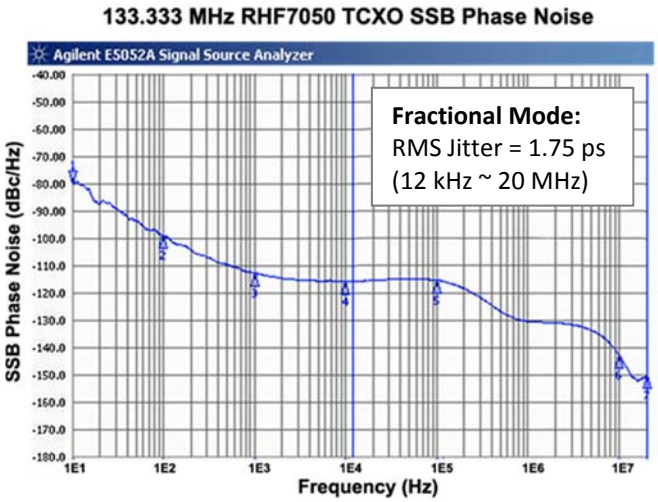
Standard Specifications

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Nominal frequency		25 – 1000		MHz	CMOS output frequency up to 180MHz
Frequency calibration			±1	ppm	Initial accuracy at 25 ± 1°C
Reflow shift			±1	ppm	Pre to post reflow ΔF (measured ≥ 60 minutes after reflow)
Operating temperature range	-40		85	°C	
Frequency stability over temperature			±0.28 – ±2.5	ppm	Reference to (Fmax + Fmin)/2. The best available stability depends on the nominal frequency and selected operating temperature range
Frequency slope			0.1	ppm/°C	Minimum of 1 frequency reading every 2°C, over the operating temperature range
Supply voltage stability			±0.1	ppm	•
Load sensitivity			±10	ppb	• HCMOS, ACMOS: ±5pF variation, • Clipped sine wave / Sine wave: ±10% variation reference to frequency at nominal load
Long term stability (ageing)			±1 ±2 ±6	ppm ppm ppm	Per 1 year Per 2 year Per 10 year
Supply voltage, V_{CC} Current (CMOS) Current (LVPECL) Current (LVDS)		3.3	 35 50 40	V mA mA mA	±5% 25 – 180MHz 25MHz – 1GHz 25MHz – 1GHz
Control voltage, Vc		1.65		V	
Frequency tuning	±3			ppm	Nominal control voltage ±1 V
VCO pin input impedance			100	kΩ	
Frequency tuning linearity			10	%	Deviation from straight line curve fit
Oscillator output (CMOS) V_{OL} V_{OH} Duty cycle	 90%V_{DD} 48		 10%V_{DD} 52	 V V %	 15pF capacity load 15pF capacity load Measured at 50% V_{DD} trigger level
Oscillator output (LVPECL) V_{OL} V_{OH} Duty cycle	 V_{DD} –1.03		 V_{DD} –1.6	 V V	 50Ω nominal load 50Ω nominal load Measured at V_{DD} –2V
Oscillator output (LVDS) Duty cycle	 48	350	 52	mV	 Measured at 1.25V

SSB Phase Noise (Typical value at 25°C)

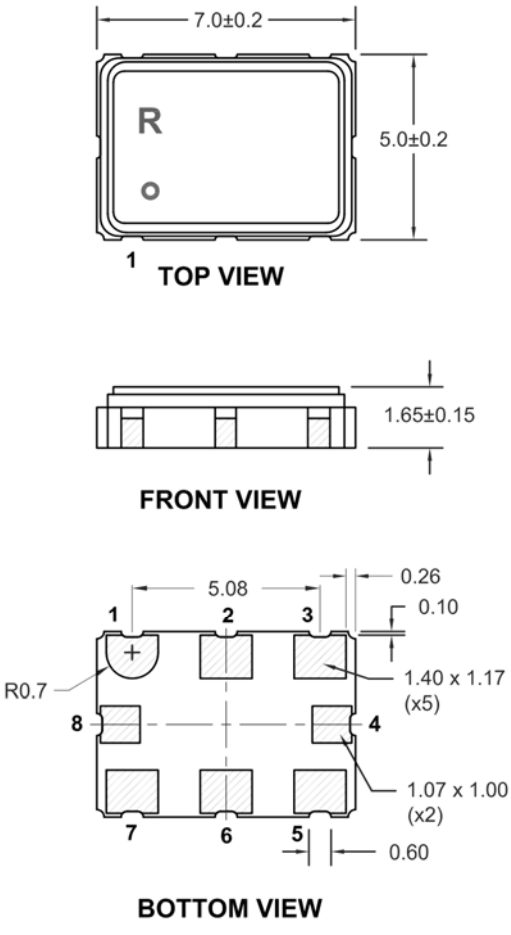


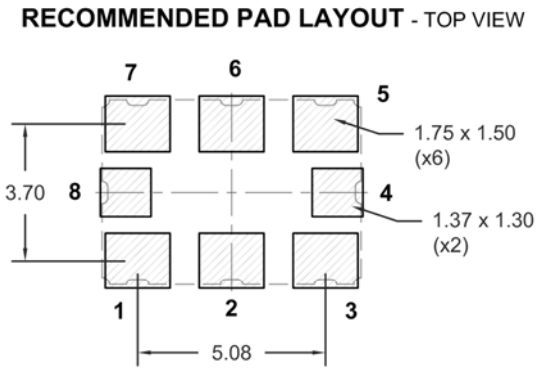
The standard frequencies as the multiples of 25 (25, 50, 100, 125, etc.)



Please send an email to Sales@rakon.com for availability of other frequencies.

Model Outline and Recommended Pad Layout





PIN CONNECTIONS

1*	Vc, NC
2*	E/D
3	GND
4	NC
5	Output
6*	Complementary Output (LVPECL/LVDS), NC
7	V_{DD}
8	NC

* Depending on the specifications

NOTE: Outline unit is mm.