Digital pulse compression module

CI F07 Dual Expander

To make an enquiry please email: info@rakon.fr

Product description

CI F07 unit includes two digital pulse expander channels housed in a single unit.

The pulse expander generates a frequency coded pulse, also called a chirp. Pulse output is IF analog.

CI F07 may be customized by Rakon to generate linear or non linear chirps.

CI F07 may be used as a replacement of existing SAW based pulse expander to overcome device obsolescence or enhance RADAR performances.

CI F07 behavior and performances are reproducible from one unit to the other. No matching is needed.

Rakon will customize pulse expander chirp according to the characteristics requested by the customer (Chirp duration, bandwidth, chirp slope …).

The unit is provided with FPGA firmware loaded, including pulse expander waveforms.

Features

- Dual channel pulse expander unit
- IF analog I/Os
- Two Selectable Waveforms for each channel
- High precision clock
- BITE function
- High Time dispersion.

Applications

- SAW based pulse compression RADARS upgrade
- FMCW RADARs

Technical description

CI F07 functional block diagram is featured on Fig. 1.

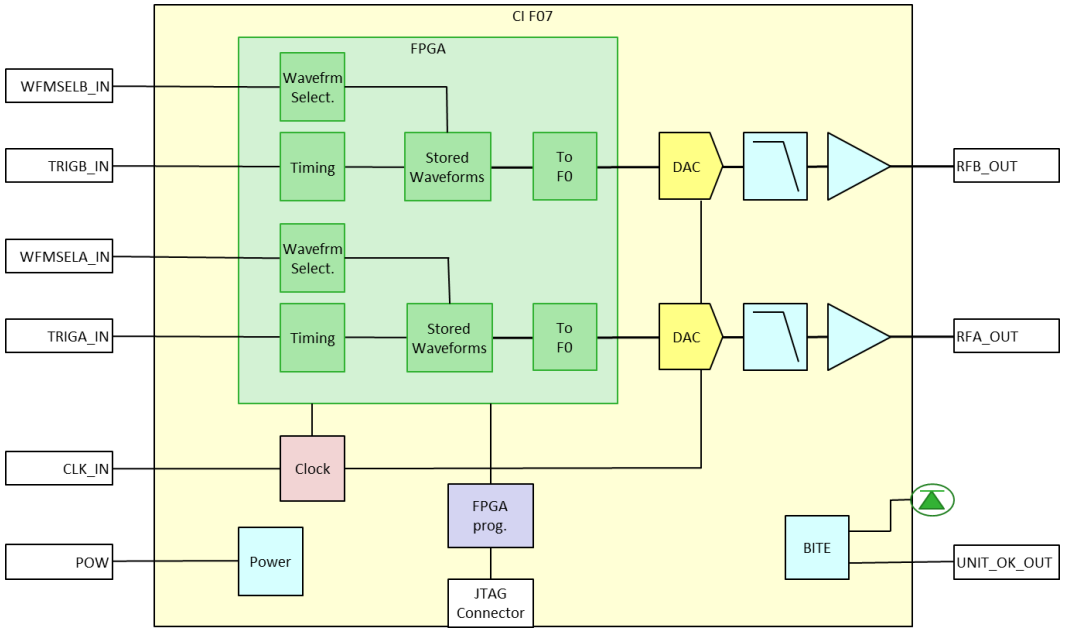

Fig. 1 : CI F07 functional block diagram

Unit description.

The internal low noise system clock is locked on an external clock (derived from the RADAR system clock). For proper operation, the clock should be a good quality clock, with a low phase noise close to the carrier.

CI F07 unit is provided with FPGA firmware loaded. Functions, and channels specifications (time dispersion, bandwidth…) should be provided by customer; Rakon will customize the FPGA program to fulfill customer requirements.

CI F07 unit continuously monitors internal power supply and FPGA program integrity. If voltage exceeds nominal levels, or if FPGA program is corrupted, UNIT_OK_OUT output is deasserted, and LED is turned off. The UNIT_OK_OUT output indicates the GO-NOGO state of the compressor.

Pulse expander channel description.

After each Trigger pulse, a chirp defined by the samples set selected by WFMSELx_IN is generated, and presented to the DAC input to be translated into an analog signal. Trigger input have to be synchronized with Clock input.

For better compatibility with old SAW based subsystems, an adjustable additional delay may be inserted.

Expander waveform is selected among 2 possible waveforms, using WFMSELx_IN input, as presented in Table 1. Each time WFMSELx_IN signal changes, the new set of waveform samples will be active for the next trigger pulse.

Table 1 : Expander Waveform Selection

WFMSELx	Expander Waveform
0	Waveform 0 (TBD)
1	Waveform 1 (TBD)

Specifications

1. Environmental conditions

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
1.1	Temperature operating		-25		+60	°C
1.2	Temperature storage		-40		+85	°C
1.3	Humidity operating	@ 30 °C, (non condensing)			95	% RH
1.4	Shock	11 ms, 3 axes, 2 dir, half sine pulse (1).			30	g
1.5	Random Vibration	20 to 500 Hz, 3 axes (1).			0.1	g^2/Hz
1.6	EMI - EMC	In accordance with MIL-STD 461 E				

Note (1) : Procedures refer to MIL-STD-810G

2. Electrical Interface

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Power supply (refers to POW)					
2.1	Voltage		11		26	V
2.2	Current	@ Power supply = 15 V		500 (1)		mA
	Clock Input (refers to CLK_IN)					
2.3	Input level		-10	0	10	dBm
2.4	Frequency		0		250	MHz
2.5	Phase noise @ 1 kHz	For a 20 MHz clock input			-130	dBc/Hz
2.6	VSWR				1.5:1	
	RF expander output signal (refers to RFA_OUT, RFB_OUT)					
2.7	Maximum output level			10		dBm
2.8	Output level variation with temperature				± 1	dB
2.9	Maximum time domain amplitude ripple			± 0.1		dB
2.10	Rise / Fall time	From 10 % to 90 % max level			50	ns
2.11	Spurious harmonic level				-70	dBc
2.12	Output noise floor	Inside chirp bandwidth		-140		dBm/Hz
2.13	Maximum phase error within the chirp			± 2		Deg.
2.14	VSWR				1.3:1	
	RS-422 control inputs (refers to TRIGA_IN, TRIGB_IN, WFMSELA_IN, WFMSELB_IN)					
2.15	Impedance			120		Ω
2.16	Setup time	To clock rising edge	50			ns
2.17	Hold time	From clock rising edge	50			ns

Note (1): Current highly depends on waveform characteristics (B, T, …)

3. CI F07 expander operation Performances

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
3.1	Center frequency (F0)				75 – B/2	MHz
3.2	Maximum bandwidth (B)			45		MHz
3.3	Maximum time dispersion (T)	@ B = 7 MHz		1000		µs
3.4	Minimal expander delay (TE)	See Note (1)		T/2 + 0.3		µs
3.5	Maximal additional expander delay (TE)	See Note (1)		1		ms
3.6	Modulation slope		Up-chirp / Down-chirp			
3.7	Modulation type		Linear / Non linear			

Note (1): Measured from first Clock rising edge after Trigger low to high transition, to the center of the output chirp.

Mechanical features

4. Mechanical features

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
4.1	Unit outline without connectors			175 x 152 x 27.1		mm^3
4.2	Unit weight			< 0.6		kg
4.3	Material			AG4.5MC		
4.4	Treatment			Ni20 / Zn1		
4.5	Screws			A4-70 stainless steel		

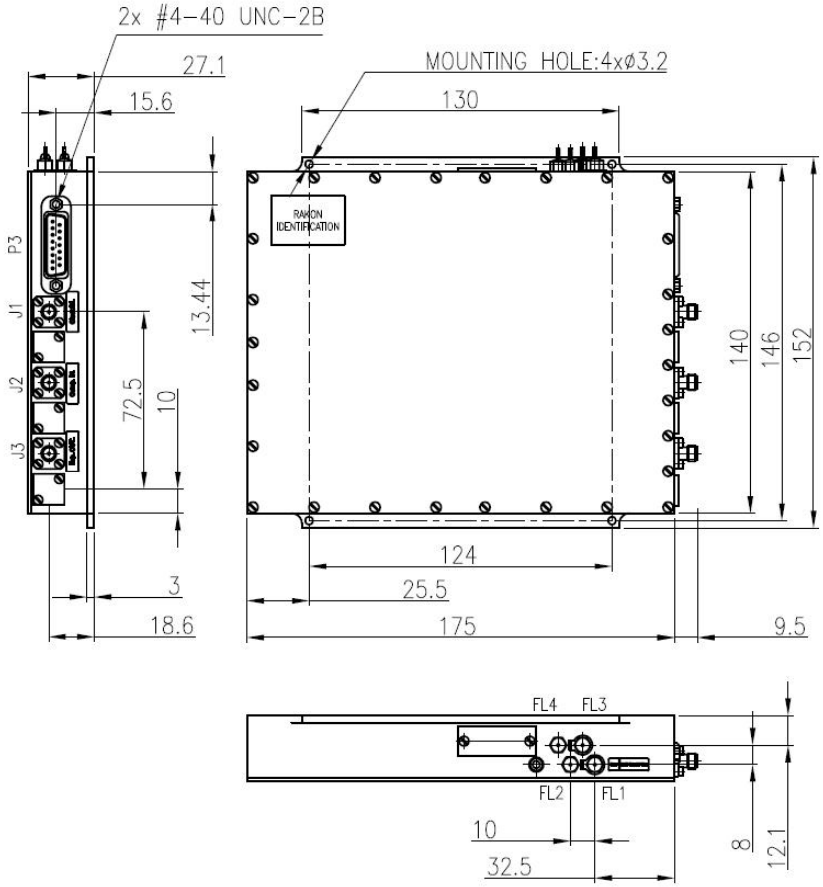

Fig. 2 : Mechanical drawing

Reliability

5. Reliability information

Line	Parameter	Test Condition	Value	Unit
5.1	Estimated mean time between failure	FIDES 2004, 30°C ambient	> 250 000	H

6. Interfaces description

Line	Pin number	Name	Description
	J1 to J3 : SMA – Jack		
6.1	J1	CLK_IN	Reference clock input AC, 50 Ω
6.2	J2	RFB_OUT	Expander channel B RF chirp output AC, 50 Ω
6.3	J3	RFA_OUT	Expander channel A RF chirp output AC, 50 Ω
	FL01 to FL04 : By-pass filter		
6.4	FL01	Power supply return	Power supply return
6.5	FL02	Power supply	Power supply
6.6	FL03	Pi filter	Not used
6.7	FL04	Pi filter	Not used
	P1 : MIL-C-24308 15-pin SubD Connector		
6.8	P1 – 4 / P1 – 12	WFMSELA_IN +/-	Expander A Waveform selection input RS-422 compatible input, 120 Ω differential impedance
6.9	P1 – 6 / P1 – 14	WFMSELB_IN +/-	Expander B Waveform selection input RS-422 compatible input, 120 Ω differential impedance
6.10	P1 – 2 / P1 – 10	TRIGA_IN +/-	Trigger A input Time reference = First clock rising edge following Trigger low to high transition. RS-422 compatible input, 120 Ω differential impedance
6.11	P1 – 3 / P1 – 11	TRIGB_IN +/-	Trigger B input Time reference = First clock rising edge following Trigger low to high transition. RS-422 compatible input, 120 Ω differential impedance
6.12	P1 – 5 / P1 – 13	UNIT_OK_OUT +/-	BITE output RS-422 level, Logic 1 = Unit OK Indicates the GO-NOGO state of the unit
6.13	P1 – 8	GND	Ground
6.14	P1 – 15	UNIT_OK_OCOUT	Open Collector BITE Output TTL Level with 300 Ω internal pull-up, Logic 1 = Unit OK Indicates the GO-NOGO state of the unit May be tied to other UNIT_OK_OCOUT to generate a global System OK when 2 or more CI F07 units are used
	P3 : MOLEX type 87833-1420		
6.15	P3	JTAG	JTAG interface for program download