Digital pulse compression module
CI E03

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Product Description

CI E03 is a digital dual pulse compression module, well suited for RADARS performance enhancement. Analog inputs and outputs make it an ideal replacement for SAW based pulse compression subsystems.

Each of the two available channels may be configured as chirp expander or chirp compressor.

All the pulse compression parameters are programmable (center frequency, bandwidth, time dispersion, modulation law, weighting function, etc.).

CI E03 is provided with FPGA firmware, which will be configured by Rakon, based on customer requirements.

Features

- Digital pulse compression module
- 2 concurrent channels : Expander or compressor for each channel
- 2 x IF analog inputs, 2 x IF analog outputs
- High precision clock, self sufficient or externally locked
- BITE function
- Low profile
- High BxT compression gain

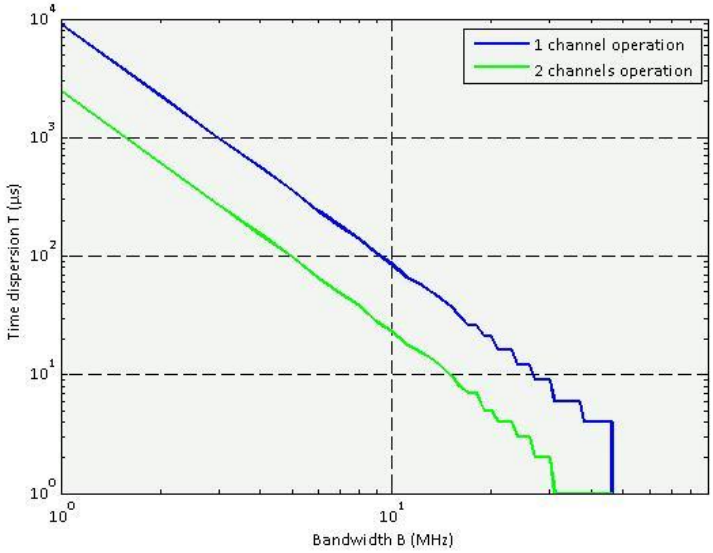

Fig. 1 : Maximum B x T compression parameters

Applications

- SAW based pulse compression RADARS upgrade

Technical description

CI E03 functional bloc diagram is featured on Fig. 2.

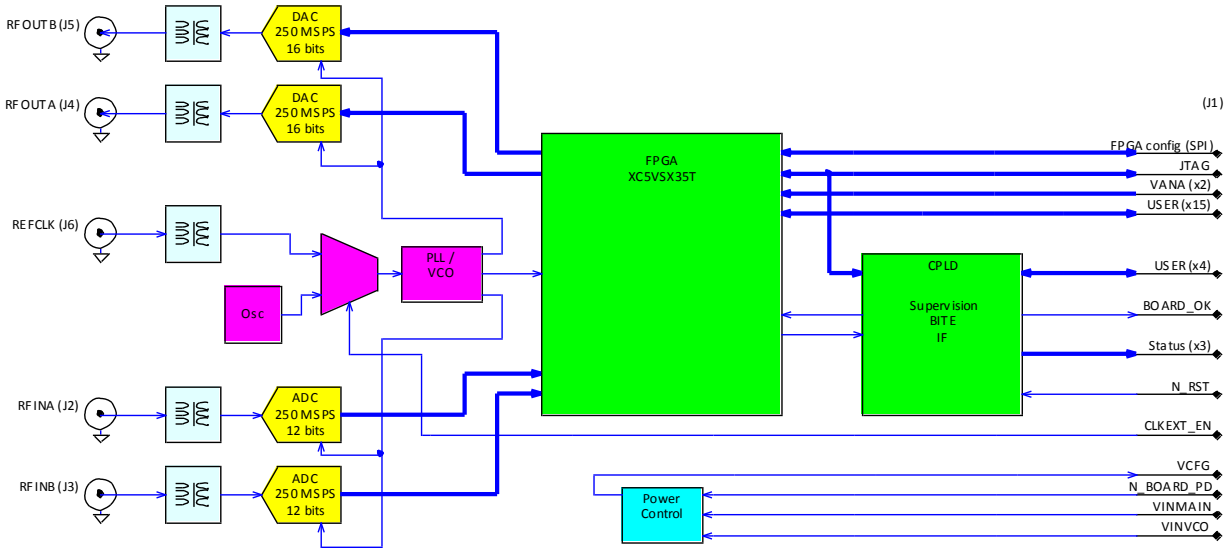

Fig. 2 : CI E03 functional bloc diagram

This module is specifically designed to upgrade existing SAW based pulse compression subsystems. Plugged on a specific carrier board, this module may upgrade many existing expanders and/or compressors. With a low size and low profile, it may be embedded in small form factors.

This module is able to process on-the-fly 2 independent and concurrent channels. Each channel may be an expander or a compressor. The two independent channels are processed in a single FPGA, but each of them uses dedicated resources.

The internal clock generator is self-sufficient but may also be locked on an external clock. An external clock is required for expander channels, but is optional for compressor channels.

As the two channels uses the same ADC, same DAC component types and the same reference clock, the phase difference will be close to 0, and will be very stable inside the operating range. There is no need to use phase shifters to adjust phase difference.

16 different waveforms, each of them with different specification, may be stored for each expander channel. The active waveform is selected with 4 user inputs on J1 connector. Expander channel waveforms allows for Doppler pre-correction, e.g. there may be 2 waveforms with different specifications, each of them with 8 different Doppler pre-corrections ranging from negative values to positive values.

FPGA firmware resides inside a flash PROM located on the carrier board, thus CI E03 has not to be application dependant; the same CI E03 board may be used without any modification or firmware upgrade for different applications. Firmware is automatically loaded in the FPGA at startup.

CI E03 module continuously monitors its internal temperature, powers off FPGA and some other components and deasserts TEMP_OK signal on J1 connector if temperature exceeds a secure maximum threshold.

CI E03 module is provided with FPGA firmware to be loaded on the carrier flash memory. Functions, and channels specifications (time dispersion, compressed pulse width, side lobes level,…) should be provided by customer; Rakon will customize the FPGA program to fulfill customer requirements.

Expander channel bloc diagram is featured in Fig. 3. After each trigger pulse, a chirp defined by the samples set selected by EXP_SELECT_x (user signals) is generated, and presented to the DAC input to be translated into an analog signal. When the control input state changes, another waveform samples set is selected, and will be active for the next trigger pulse.

For better compatibility with old SAW based subsystems, an adjustable additional delay may be inserted.

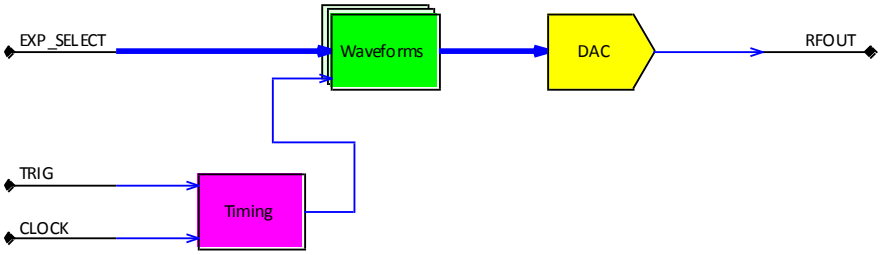

Fig. 3 : Expander channel bloc diagram

Compressor, featured in Fig. 4, uses a FIR filter whose coefficients are matched to the expander waveform samples. Input data are preliminary translated into baseband, and then are translated again into IF signal. Digital IF signal is then presented to the DAC to be translated into an analog IF signal.

For better compatibility with old SAW based subsystems, an adjustable additional delay may be inserted.

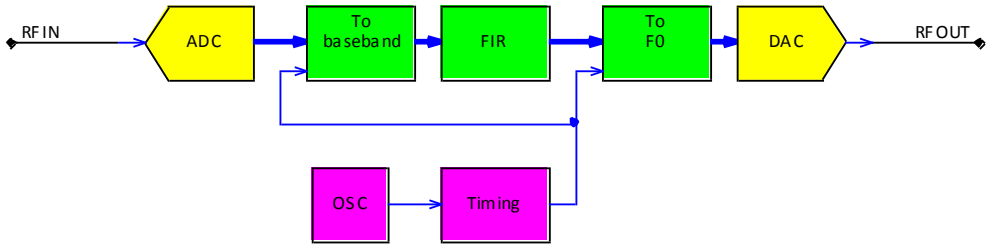

Fig. 4 : Compressor channel bloc diagram

Fig. 5 represents the maximum time dispersion vs. bandwidth area covered with one and two concurrent compressor channels operating. These areas assume 250 MHz internal clock, and a compressor sample period of ζ_{-3dB} / 3.5. Contact Rakon-Temex form higher Time x Bandwidth products.

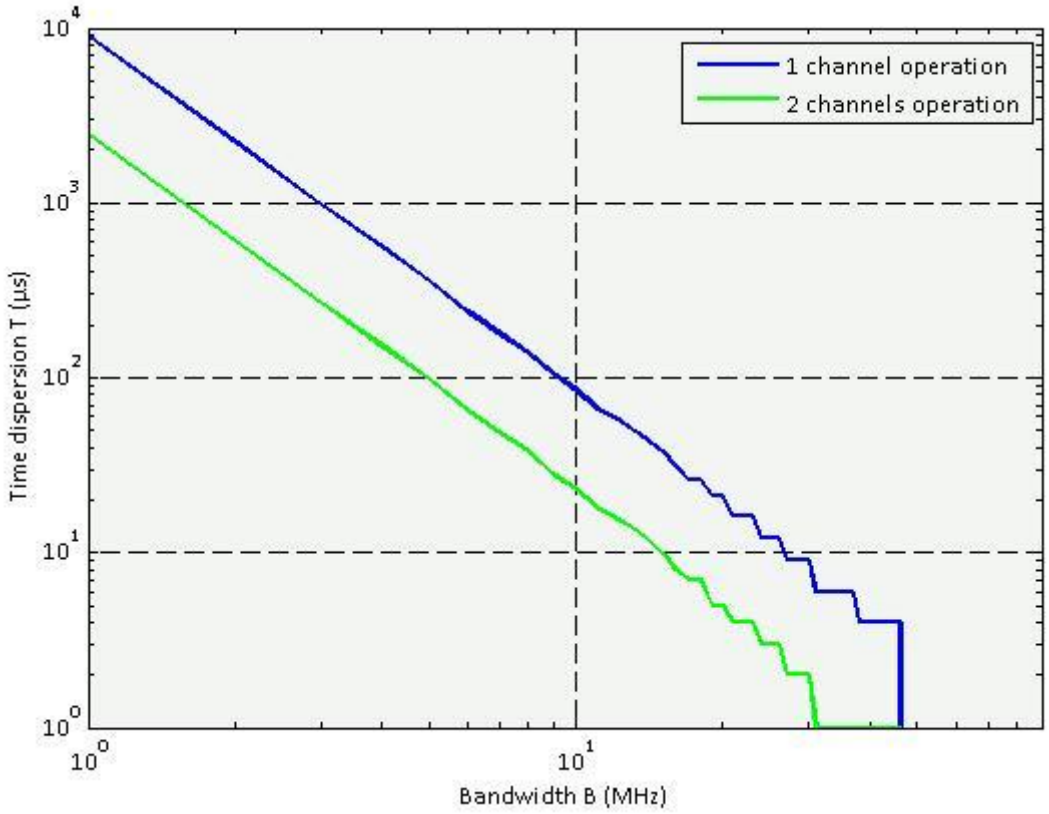

Fig. 5 : Maximum Time dispersion vs. Bandwidth

Specifications

1.0 Environmental conditions

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Operating temperature range					
1.1	Forced air cooling (250 ft/min at sea level)	VITA 47 Class AC2, FC2	-40		+55	°C
1.2	Conduction cooling with specific heat sink	VITA 47 Class CC3	-40		+70	°C
1.3	Storage temperature range	VITA 47 Class C2	-40		+85	°C
1.4	Humidity	30 °C (non condensing)			95	% RH
	Vibration					
1.5	PSD (5 Hz to 100 Hz)	VITA 47 Class V2	increasing at 3 dB/octave			g^2/Hz
1.6	PSD (100 Hz ~ 1000 Hz)	VITA 47 Class V2	0.04			g^2/Hz
1.7	PSD (100 Hz ~ 1000 Hz)	VITA 47 Class V2	decreasing at 6 dB/octave			g^2/Hz
1.8	Shock	VITA 47, Class OS1			20	g

2.0 Electrical Interface

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Power supply					
2.1	Voltage		5.5		13.2	V
2.2	Power dissipation [1]	1 or 2 expander channels operation		5	10	W
2.3	Power dissipation [1]	1 compressor channel operation		8	15	W
2.4	Power dissipation [1]	2 compressor channels operation		9.5	15	W
	RF_IN_A / RF_IN_B					
2.5	Coupling			AC		
2.6	Impedance			50		Ω
2.7	Sampling rate				250	MSPS
2.8	Resolution			12		bits
2.9	Bandwidth				100	MHz
2.10	Input level				8	dBm

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	RF_OUT_A / RF_OUT_B					
2.11	Coupling			AC		
2.12	Impedance			50		Ω
2.13	Sampling rate				250	MSPS
2.14	Resolution			16		bits
2.15	Bandwidth				100	MHz
2.16	Output level				5	dBm
	CLK_IN					
2.17	Coupling			AC		
2.18	Impedance			50		Ω
2.19	Frequency		10	20[2]	125	MHz
	Status signals (BOARD_OK, INITTIME_ALM, POWER_OK, TEMP_OK)					
2.20	Logic high output voltage	IOH = 8 mA	2.9		3.3	V
2.21	Logic low output voltage	IOL = 8 mA	0		0.4	V
	Control signals (CLKEXT_EN, N_RST)					
2.22	Logic high input voltage		2.0		3.3	V
2.23	Logic low input voltage		0		0.8	V
	Power down signal (N_BOARD_PD)					
2.24	Logic low input voltage		0		1	V
	User signals (USERCLVTx)					
2.25	Logic high input voltage		2.0		3.3	V
2.26	Logic low input voltage		0		0.8	V
2.27	Logic high output voltage	IOH = 8 mA	2.9		3.3	V
2.28	Logic low output voltage	IOL = 8 mA	0		0.4	V
	User signals (USERFLVTx)					
2.29	Logic high input voltage		2.0		3.3	V
2.30	Logic low input voltage		0		0.8	V
2.31	Logic high output voltage	IOH = 2 to 24 mA (programmable)	2.4		3.3	V
2.32	Logic low output voltage	IOL = 2 to 24 mA (programmable)	0		0.4	V
	User signals (USERFDIFFx, programmed as single 2.5V LVCMOS signals)					
2.33	Logic high input voltage		1.7		2.5	V
2.34	Logic low input voltage		0		0.7	V
2.35	Logic high output voltage	IOH = 2 to 24 mA (programmable)	2.1		2.5	V

2.36		Logic low output voltage	IOL = 2 to 24 mA (programmable)	0		0.4	V

1 Power dissipation highly depends on channels specifications. Typical figures are given as a rough guide.
[2] Frequency should be divisible by 10 MHz

3.0 Expander operation Performances

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
3.1	Stored waveforms				16	
3.2	Center frequency (F0) [3]				100 – B/2	MHz
3.3	Bandwidth (B)				100	MHz
	Time dispersion (T)					
3.4	16 Exp Wve for each channel	2 expander channels operation			25	µs
3.5	1 Exp Wve for each channel	2 expander channels operation			400	µs
3.6	Minimal Expander delay (TE) [4]	Measured from the trigger input rising edge to the center of the output chirp		T/2 + 0.3		µs
3.7	Additional Expander delay (TE)	Measured from the trigger input rising edge to the center of the output chirp			1	s
3.8	Modulation slope		Up-chirp / Down-chirp			
3.9	Modulation Type		Linear / Non linear			

3 Some frequency values are not allowed. Center frequency should be related to the master clock by a fractional number.
4 Minimal delay depends slightly on the design. The typical figure is given as a rough guide.

4.0 Compressor operation Performances

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
4.1	Center frequency (F0) [5]				100 – B/2	MHz
4.2	Bandwidth (B)				46.9	MHz
	Time dispersion (T)					
4.3	B < 3 MHz	2 compressor operation [6]			267	µs
4.4	B < 7 MHz	2 compressor operation [6]			48	µs
4.5	B < 20 MHz	2 compressor operation [6]			5	µs
4.6	B < 7 MHz	1 compressor operation [6]			178	µs
4.7	B < 20 MHz	1 compressor operation [6]			21	µs
4.8	Compressed pulse width @ -3 dB (τ_{-3dB})		18			ns
4.9	Side lobe level (SLL) [7]			35 to 45		dB
4.10	Minimal Compressor delay (TC) [8, 9]	Measured from the center of the input chirp, to the center of the compressed pulse output		T/2 + 2.5		µs
4.11	Additional Compressor delay (TC) [9]	Measured from the center of the input chirp, to the center of the compressed pulse output			5	ms
4.12	Modulation slope		Up-chirp / Down-chirp			
4.13	Modulation type		Linear / Non linear			

5 Some frequency values are not allowed. Center frequency should be related to the master clock by a fractional number.
6 Assuming 250 MHz FPGA processing, 3.5 points inside the compressed pulse width @ -3dB.
7 Side lobe level depends on B, T and other programmable parameters. Higher values are achievable.
8 Minimal delay depends slightly on the design. The typical figure is given as a rough guide.
9 Assuming B < 7 MHz.

Mechanical features

5.0 Mechanical features

Line	Parameter	Test Condition	Value	Unit
5.1	Module size		75 x 120	mm^2
5.2	Module height	Measured from the upper side of the carrier board	10	mm
5.3	Stacking height		6.4	mm

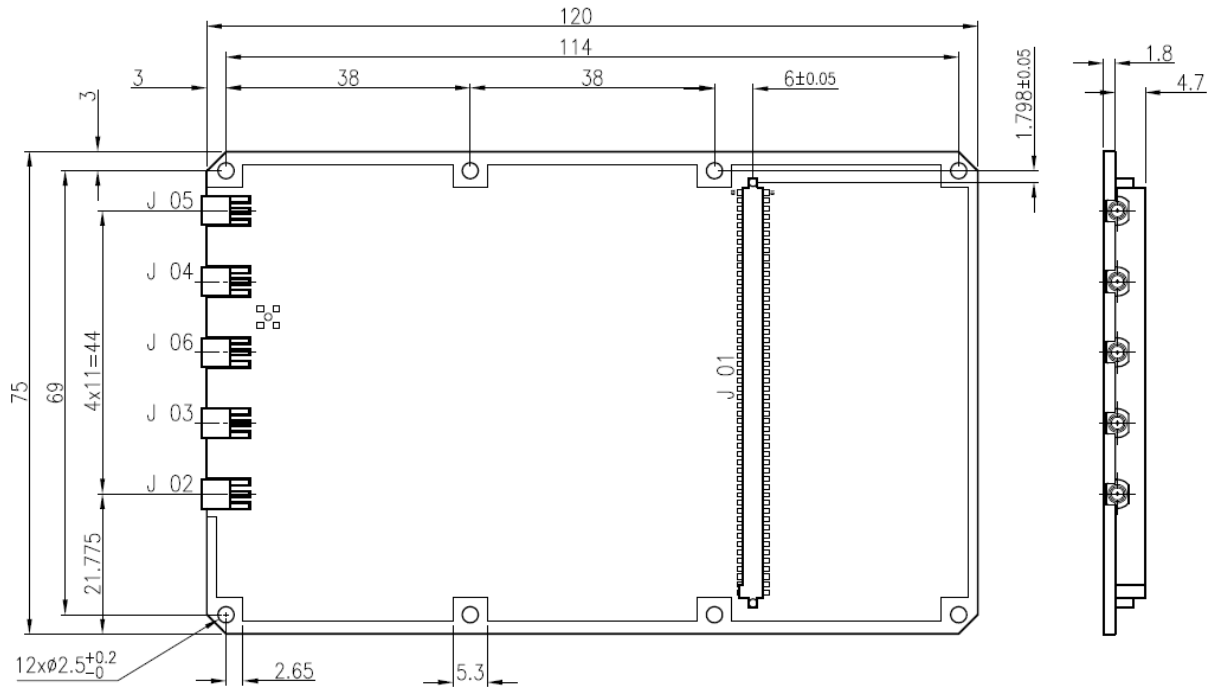

Fig. 6 : CI E03 interfaces drawing

Interfaces description

J1 : Low profile 1.27 pitch, 2x50 pins connector

J2 to J6 : MMCX jack connectors

6.0 Interfaces description

Line	Pin number	Name	Description
6.1	P1-76	BOARD_OK	Board status correct output
6.2	P1-56	CFGCCLK	FPGA configuration Clock output
6.3	P1-60	CFGCEO	FPGA configuration PROM counter input
6.4	P1-50	CFGDIN	FPGA configuration Data input
6.5	P1-48	CFGDONE	FPGA configuration termination signal output
6.6	P1-78	CLKEXT_EN	Enable external reference clock input
6.7	P1-70	INITTIME_ALM	FPGA configuration time exceeded output
6.8	P1-96	JTAGTCK	JTAG Clock input
6.9	P1-90	JTAGTDI	JTAG Data input
6.10	P1-92	JTAGTDO	JTAG Data output
6.11	P1-86	JTAGTMS	JTAG Test Mode select input
6.12	P1-100	JTAG_EN	JTAG clock buffer enable input
6.13	P1-93	N_BOARD_PD	Board power down, active low open-drain input / output with internal pull-up. Should not be driven with a logic high level.
6.14	P1-50	N_CFGINIT	FPGA configuration init signal, active low output
6.15	P1-52	N_CFGPROG	FPGA configuration program signal, active low output
6.16	P1-82	N_RST	Board active low reset input
6.17	P1-74	POWER_OK	Board power status output
6.18	P1-72	TEMP_OK	Board temperature status output
6.19	P1-68; 66; 64; 62	USERCLVT[3:0]	LVTTL user signals Each signal may be programmed independently as input or output May be used for waveform selection or other purpose
6.20	P1-30; 26; 22; 18; 14 (+) P1-28; 24; 20; 16; 12 (-)	USERFDIFF[4:0]±	Differential LVDS user signals Each pair may be programmed independently as input or output These signal may also be used as 2.5V LVCMOS single inputs or outputs
6.21	P1-10; 8; 6; 4; 2	USERFLVT[4:0]	LVTTL user signals Each signal may be programmed independently as input or output May be used for trigger input, waveform selection, or other purpose

6.22	P1-34; 42 (+) P1-36; 40 (-)	VANA[1:0]±	Low frequency differential analog input |VANAx+ - VANAx-| ≤ 1Vpp 0 ≤ VANAx- ≤ 0.5V May be used for current measurement, RF power measurement, or other purpose
6.23	P1-59	RFU	Reserved for future use
6.24	P1-11; 13; 15	VCFG	2.5V Power supply output for FPGA configuration flash PROM
6.25	P1-45; 47; 49; 51; 65; 67; 69; 71; 73; 75; 77	VINMAIN	Main power input 5.5 to 13.2 V
6.26	P1-89; 91	VINVCO	System clock power input 5.5 to 13.2 V / 30 mA
6.27	P1-1; 3; 5; 7; 9; 17; 19; 21; 23; 25; 27; 29; 31; 32; 33; 35; 37; 38; 39; 41; 43; 44; 53; 54; 55; 57; 58; 61; 63; 79; 80; 81; 83; 84; 85; 87; 88; 94; 95; 97; 98; 99	GNDD	Digital ground
6.28	J6	REFCLK	External clock input AC, 50 ohms, 0 dBm typ
6.29	J2	RFINA	Channel A input AC, 50 ohms, 8 dBm max
6.30	J3	RFINB	Channel B input AC, 50 ohms, 8 dBm max
6.31	J4	RFOUTA	Channel A output AC, 50 ohms, 5 dBm max
6.32	J5	RFOUTB	Channel B output AC, 50 ohms, 5 dBm max